

## LMC6482 CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

Check for Samples: [LMC6482](#)

### FEATURES

- (Typical Unless Otherwise Noted)
- Rail-to-Rail Input Common-Mode Voltage Range (Ensured Over Temperature)
- Rail-to-Rail Output Swing (within 20mV of Supply Rail, 100k $\Omega$  Load)
- Ensured 3V, 5V and 15V Performance
- Excellent CMRR and PSRR: 82dB
- Ultra Low Input Current: 20fA
- High Voltage Gain ( $R_L = 500k\Omega$ ): 130dB
- Specified for 2k $\Omega$  and 600 $\Omega$  Loads
- Available in VSSOP Package

### APPLICATIONS

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

### DESCRIPTION

The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

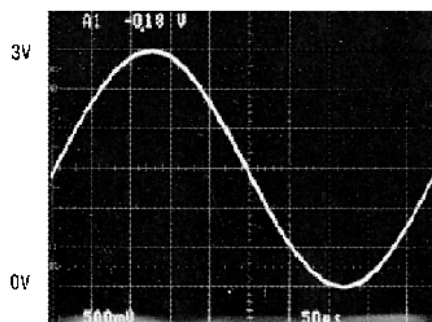
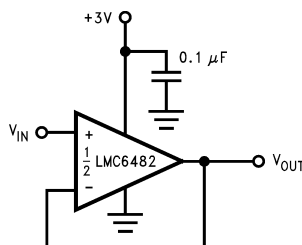
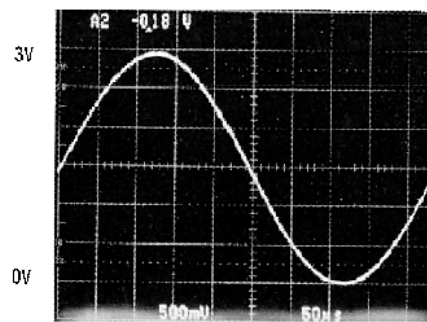
Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482's rail-to-rail output swing. The LMC6482's rail-to-rail output swing is ensured for loads down to 600 $\Omega$ .

Ensured low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

LMC6482 is also available in VSSOP package which is almost half the size of a SOIC-8 device.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

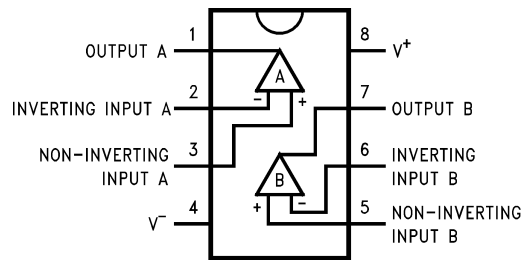
### 3V Single Supply Buffer Circuit


**Figure 1. Rail-To-Rail Input**

**Figure 2.**

**Figure 3. Rail-To-Rail Output**


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## Connection Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	1.5kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V <sup>+</sup> ) +0.3V, (V <sup>-</sup> ) -0.3V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	16V
Current at Input Pin <sup>(4)</sup>	±5mA
Current at Output Pin <sup>(5)(6)</sup>	±30mA
Current at Power Supply Pin	40mA
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature <sup>(7)</sup>	150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human body model, 1.5kΩ in series with 100pF. All pins rated per method 3015.6 of MIL-STD-883. This is a Class 1 device rating.
- (4) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
- (6) Do not short circuit output to V<sup>+</sup>, when V<sup>+</sup> is greater than 13V or reliability will be adversely affected.
- (7) The maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly into a PC board.

## Operating Ratings

Supply Voltage	3.0V ≤ V <sub>+</sub> ≤ 15.5V
Junction Temperature Range	
LMC6482AM	-55°C ≤ T <sub>J</sub> ≤ +125°C
LMC6482AI, LMC6482I	-40°C ≤ T <sub>J</sub> ≤ +85°C
Thermal Resistance (θ <sub>JA</sub> )	
P0008E Package, 8-Pin PDIP	90°C/W
D0008A Package, 8-Pin SOIC	155°C/W
DGK0008A Package, 8-Pin VSSOP	194°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

## DC Electrical Characteristics

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ (1)	LMC6482AI	LMC6482I	LMC6482M	Units	
				Limit (2)	Limit (2)	Limit (2)		
$V_{\text{OS}}$	Input Offset Voltage		0.11	0.750	3.0	3.0	mV	
				<b>1.35</b>	<b>3.7</b>	<b>3.8</b>	max	
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift		1.0				$\mu\text{V}/^\circ\text{C}$	
$I_B$	Input Current	(3)	0.02	<b>4.0</b>	<b>4.0</b>	<b>10.0</b>	pA	
							max	
$I_{\text{OS}}$	Input Offset Current	(3)	0.01	<b>2.0</b>	<b>2.0</b>	<b>5.0</b>	pA	
							max	
$C_{\text{IN}}$	Common-Mode Input Capacitance		3				pF	
$R_{\text{IN}}$	Input Resistance		>10				Tera $\Omega$	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 15.0\text{V}$ $V^+ = 15\text{V}$	82	70	65	65	dB min	
				<b>67</b>	<b>62</b>	<b>60</b>		
		$0\text{V} \leq V_{\text{CM}} \leq 5.0\text{V}$ $V^+ = 5\text{V}$	82	70	65	65	dB min	
				<b>67</b>	<b>62</b>	<b>60</b>		
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 15\text{V}$ , $V^- = 0\text{V}$ $V_O = 2.5\text{V}$	82	70	65	65	dB min	
				<b>67</b>	<b>62</b>	<b>60</b>		
-PSRR	Negative Power Supply Rejection Ratio	$-5\text{V} \leq V^- \leq -15\text{V}$ , $V^+ = 0\text{V}$ $V_O = -2.5\text{V}$	82	70	65	65	dB min	
				<b>67</b>	<b>62</b>	<b>60</b>		
$V_{\text{CM}}$	Input Common-Mode Voltage Range	$V^+ = 5\text{V}$ and $15\text{V}$ For CMRR $\geq 50\text{dB}$	$V^- - 0.3$	- 0.25	- 0.25	- 0.25	V	
				<b>0</b>	<b>0</b>	<b>0</b>	max	
			$V^+ + 0.3\text{V}$	$V^+ + 0.25$	$V^+ + 0.25$	$V^+ + 0.25$	V	
				<b><math>V^+</math></b>	<b><math>V^+</math></b>	<b><math>V^+</math></b>	min	
$A_V$	Large Signal Voltage Gain	$R_L = 2\text{k}\Omega$ (4) (5)	Sourcing	666	140	120	120	V/mV
					<b>84</b>	<b>72</b>	<b>60</b>	min
			Sinking	75	35	35	35	V/mV
					<b>20</b>	<b>20</b>	<b>18</b>	min
		$R_L = 600\Omega$ (4) (5)	Sourcing	300	80	50	50	V/mV
					<b>48</b>	<b>30</b>	<b>25</b>	min
			Sinking	35	20	15	15	V/mV
					<b>13</b>	<b>10</b>	<b>8</b>	min

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Ensured limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

(4)  $V^+ = 15\text{V}$ ,  $V_{\text{CM}} = 7.5\text{V}$  and  $R_L$  connected to  $7.5\text{V}$ . For Sourcing tests,  $7.5\text{V} \leq V_O \leq 11.5\text{V}$ . For Sinking tests,  $3.5\text{V} \leq V_O \leq 7.5\text{V}$ .

(5) Ensured limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

## DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ (1)	LMC6482AI	LMC6482I	LMC6482M	Units	
				Limit (2)	Limit (2)	Limit (2)		
$V_O$	Output Swing	$V^+ = 5\text{V}$ $R_L = 2\text{k}\Omega$ to $V^+/2$	4.9	4.8	4.8	4.8	V	
			<b>4.7</b>	<b>4.7</b>	<b>4.7</b>	min		
			0.1	0.18	0.18	0.18	V	
			<b>0.24</b>	<b>0.24</b>	<b>0.24</b>	max		
			$V^+ = 5\text{V}$ $R_L = 600\Omega$ to $V^+/2$	4.7	4.5	4.5	4.5	V
				<b>4.24</b>	<b>4.24</b>	<b>4.24</b>	min	
		0.3		0.5	0.5	0.5	V	
		$V^+ = 15\text{V}$ $R_L = 2\text{k}\Omega$ to $V^+/2$	14.7	14.4	14.4	14.4	V	
			<b>14.2</b>	<b>14.2</b>	<b>14.2</b>	min		
			0.16	0.32	0.32	0.32	V	
		$V^+ = 15\text{V}$ $R_L = 600\Omega$ to $V^+/2$	14.1	13.4	13.4	13.4	V	
			<b>13.0</b>	<b>13.0</b>	<b>13.0</b>	min		
0.5	1.0		1.0	1.0	V			
$I_{\text{SC}}$	Output Short Circuit Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	20	16	16	16	mA	
			<b>12</b>	<b>12</b>	<b>10</b>	min		
		Sinking, $V_O = 5\text{V}$	15	11	11	11	mA	
$I_{\text{SC}}$	Output Short Circuit Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	30	28	28	28	mA	
			<b>22</b>	<b>22</b>	<b>20</b>	min		
		Sinking, $V_O = 12\text{V}$ (6)	30	30	30	30	mA	
$I_S$	Supply Current	Both Amplifiers $V^+ = +5\text{V}$ , $V_O = V^+/2$	1.0	1.4	1.4	1.4	mA	
			<b>1.8</b>	<b>1.8</b>	<b>1.9</b>	max		
		Both Amplifiers $V^+ = 15\text{V}$ , $V_O = V^+/2$	1.3	1.6	1.6	1.6	mA	
			<b>1.9</b>	<b>1.9</b>	<b>2.0</b>	max		

(6) Do not short circuit output to  $V^+$ , when  $V^+$  is greater than 13V or reliability will be adversely affected.

## AC Electrical Characteristics

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ , and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ (1)	LMC6482AI	LMC6482I	LMC6482M	Units
				Limit (2)	Limit (2)	Limit (2)	
SR	Slew Rate	(3)	1.3	1.0	0.9	0.9	V/ $\mu\text{s}$
				<b>0.7</b>	<b>0.63</b>	<b>0.54</b>	min
GBW	Gain-Bandwidth Product	$V^+ = 15\text{V}$	1.5				MHz
$\phi_m$	Phase Margin		50				Deg

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3)  $V^+ = 15\text{V}$ . Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

### AC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ , and  $R_L > 1\text{M}$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ (1)	LMC6482AI	LMC6482I	LMC6482M	Units
				Limit (2)	Limit (2)	Limit (2)	
$G_m$	Gain Margin		15				dB
	Amp-to-Amp Isolation	(4)	150				dB
$e_n$	Input-Referred Voltage Noise	$F = 1\text{kHz}$ $V_{\text{cm}} = 1\text{V}$	37				$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$F = 1\text{kHz}$	0.03				$\text{pA}/\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	$F = 10\text{kHz}$ , $A_V = -2$ $R_L = 10\text{k}\Omega$ , $V_O = 4.1 V_{\text{PP}}$	0.01				%
		$F = 10\text{kHz}$ , $A_V = -2$ $R_L = 10\text{k}\Omega$ , $V_O = 8.5 V_{\text{PP}}$ $V^+ = 10\text{V}$	0.01				%

(4) Input referred,  $V^+ = 15\text{V}$  and  $R_L = 100\text{ k}\Omega$  connected to  $7.5\text{V}$ . Each amp excited in turn with  $1\text{ kHz}$  to produce  $V_O = 12 V_{\text{PP}}$ .

### DC Electrical Characteristics

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{M}$ .

Parameter		Test Conditions	Typ (1)	LMC6482AI	LMC6482I	LMC6482M	Units
				Limit (2)	Limit (2)	Limit (2)	
$V_{\text{OS}}$	Input Offset Voltage		0.9	2.0	3.0	3.0	mV
				<b>2.7</b>	<b>3.7</b>	<b>3.8</b>	max
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift		2.0				$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		0.02				pA
$I_{\text{OS}}$	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 3\text{V}$	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	$3\text{V} \leq V^+ \leq 15\text{V}$ , $V^- = 0\text{V}$	80	68	60	60	dB min
$V_{\text{CM}}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{dB}$	$V^- - 0.25$	0	0	0	V max
			$V^+ + 0.25$	$V^+$	$V^+$	$V^+$	V min
$V_O$	Output Swing	$R_L = 2\text{k}\Omega$ to $V^+/2$	2.8				V
			0.2				V
		$R_L = 600\Omega$ to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
$I_S$	Supply Current	Both Amplifiers	0.825	1.2	1.2	1.2	mA
				<b>1.5</b>	<b>1.5</b>	<b>1.6</b>	max

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

## AC Electrical Characteristics

Unless otherwise specified,  $V^+ = 3V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$ , and  $R_L > 1M$ .

Parameter		Test Conditions	Typ <sup>(1)</sup>	LMC6482AI	LMC6482I	LMC6482M	Units
				Limit <sup>(2)</sup>	Limit <sup>(2)</sup>	Limit <sup>(2)</sup>	
SR	Slew Rate	<sup>(3)</sup>	0.9				V/ $\mu$ s
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	F = 10kHz, $A_V = -2$ $R_L = 10k\Omega$ , $V_O = 2 V_{PP}$	0.01				%

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Connected as voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

### Typical Performance Characteristics

$V_S = +15V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

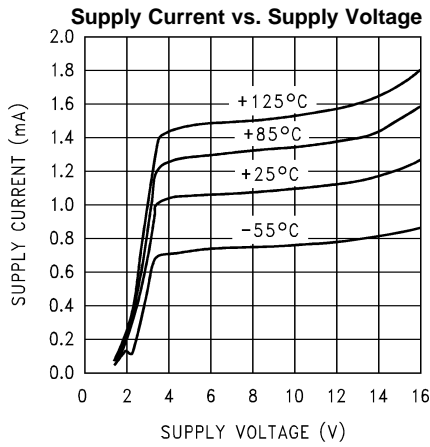


Figure 4.

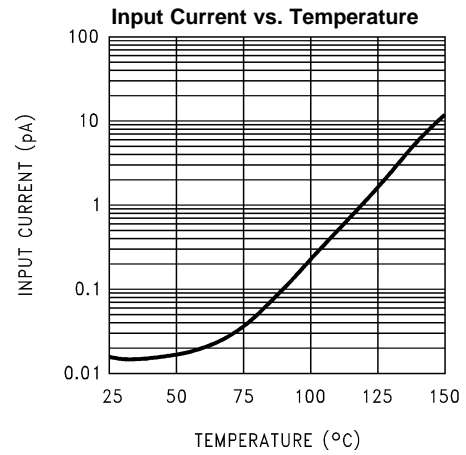


Figure 5.

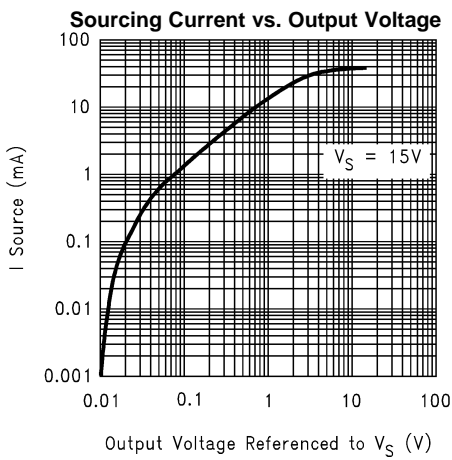


Figure 6.

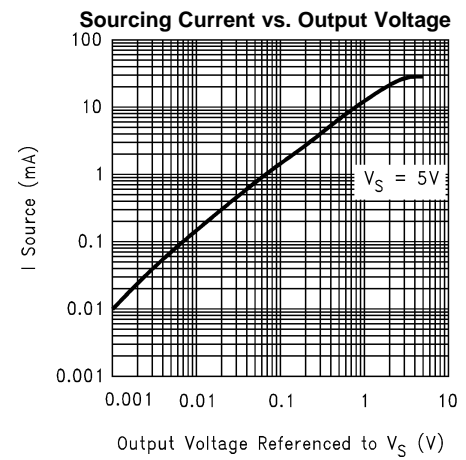


Figure 7.

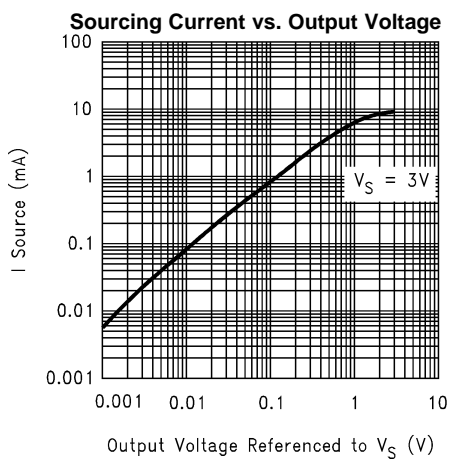


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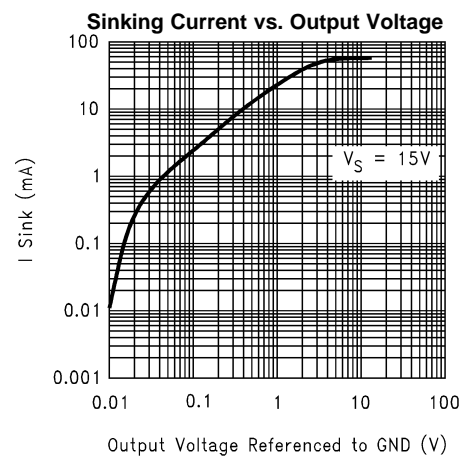
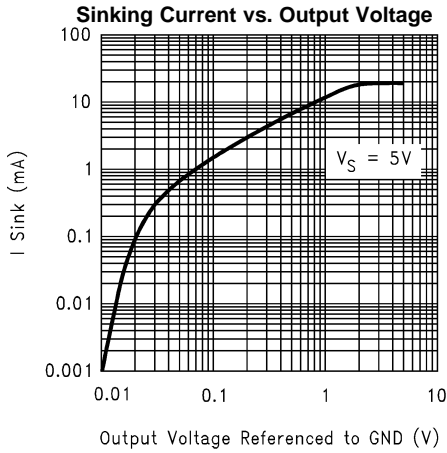


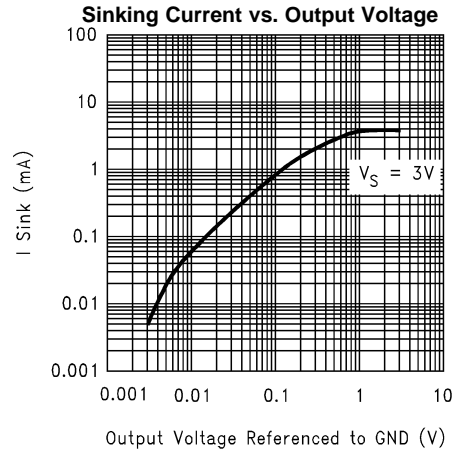
Figure 9.

**Typical Performance Characteristics (continued)**

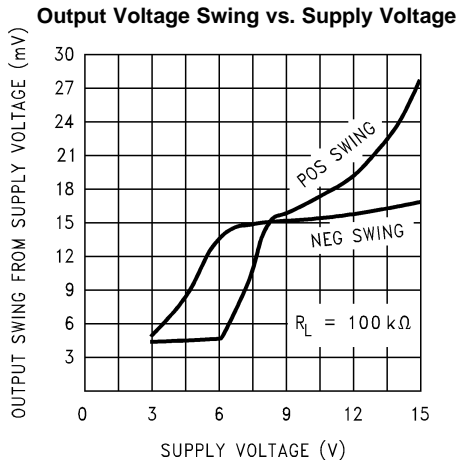
$V_S = +15V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified



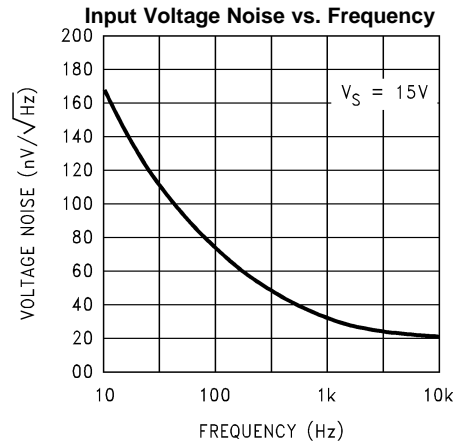
**Figure 10.**



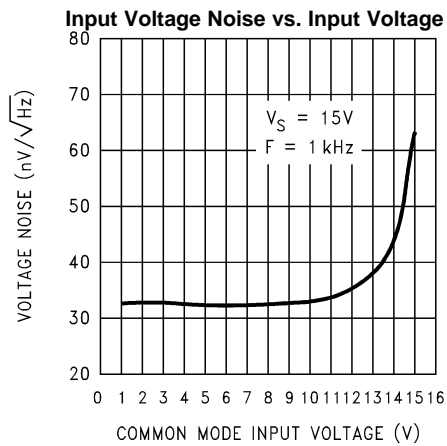
**Figure 11.**



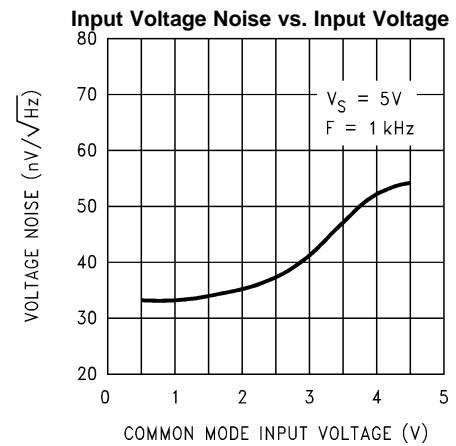
**Figure 12.**



**Figure 13.**



**Figure 14.**



**Figure 15.**



Typical Performance Characteristics (continued)

$V_S = +15V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

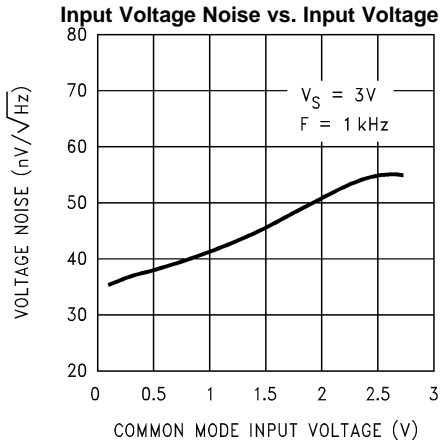


Figure 16.

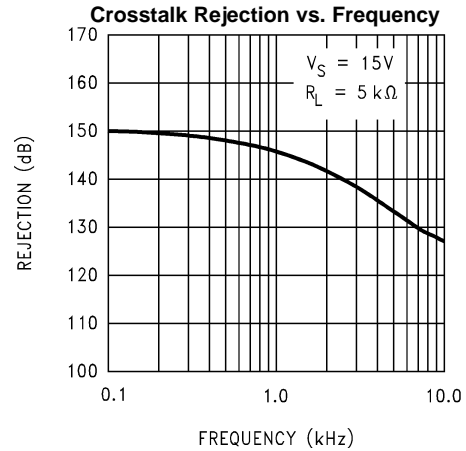


Figure 17.

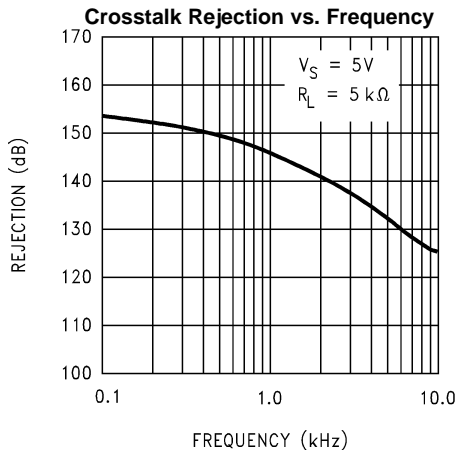


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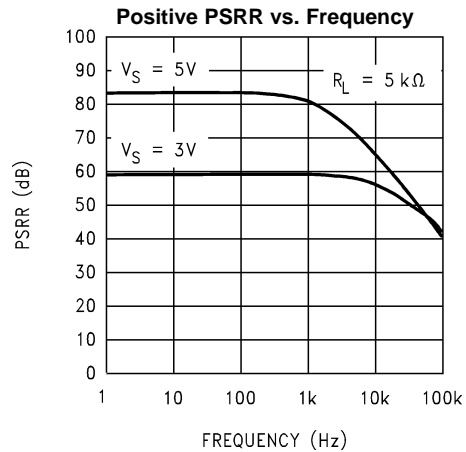


Figure 19.

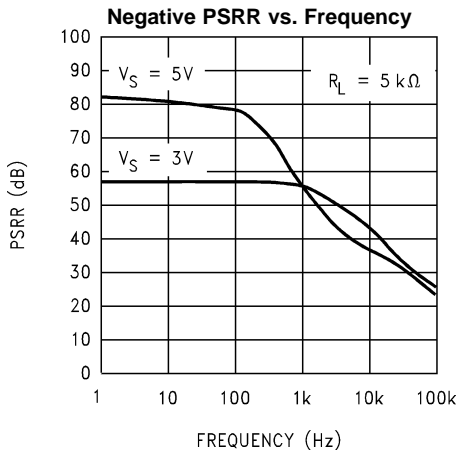


Figure 20.

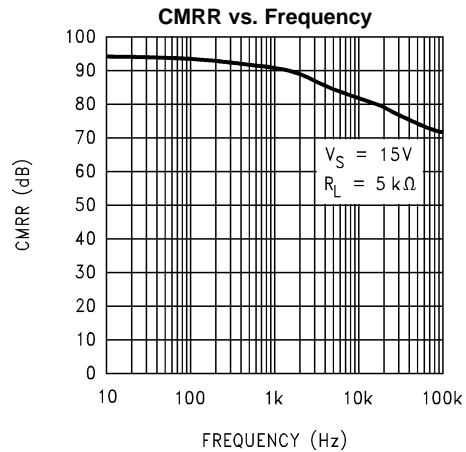


Figure 21.

Typical Performance Characteristics (continued)

$V_S = +15V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

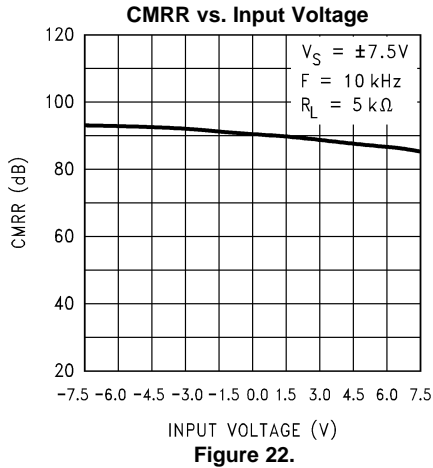


Figure 22.

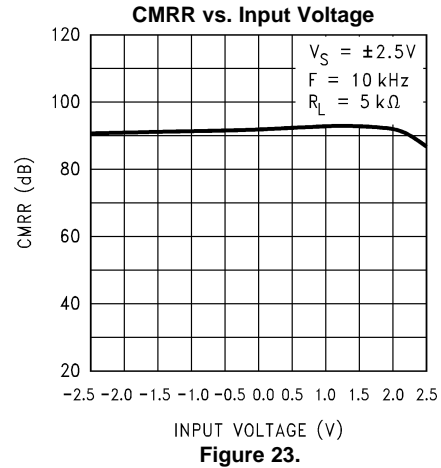


Figure 23.

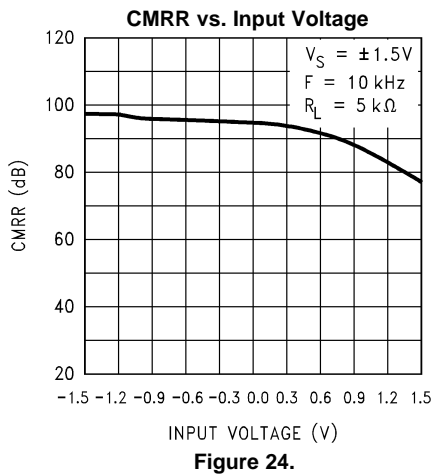


Figure 24.

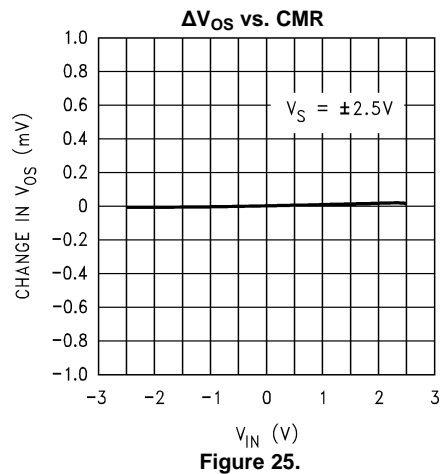


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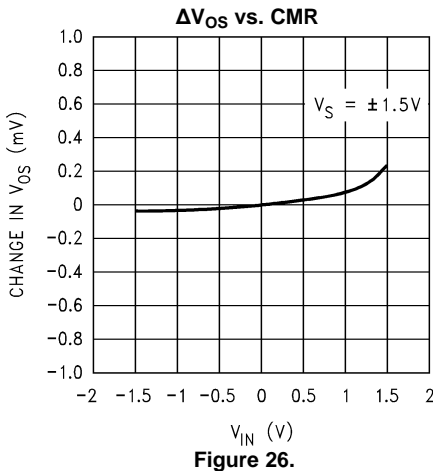


Figure 26.

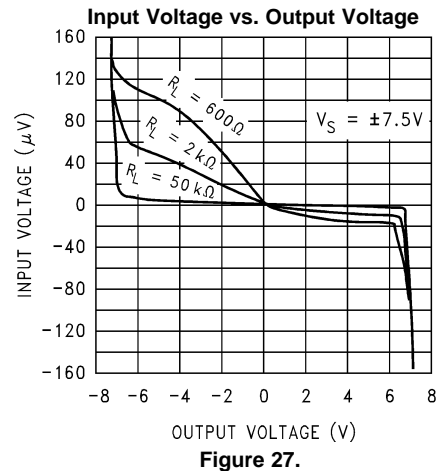


Figure 27.

Typical Performance Characteristics (continued)

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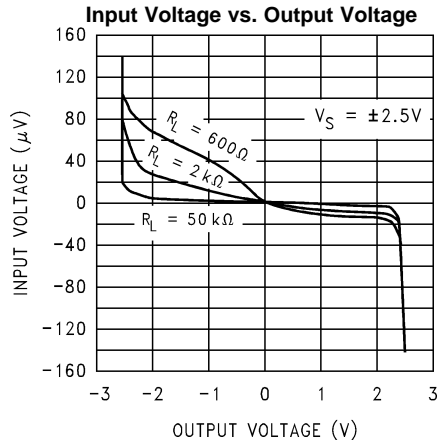


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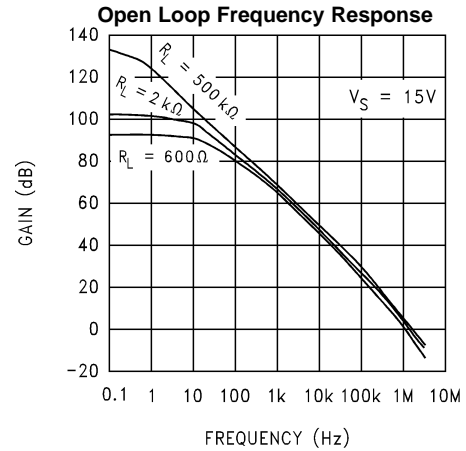


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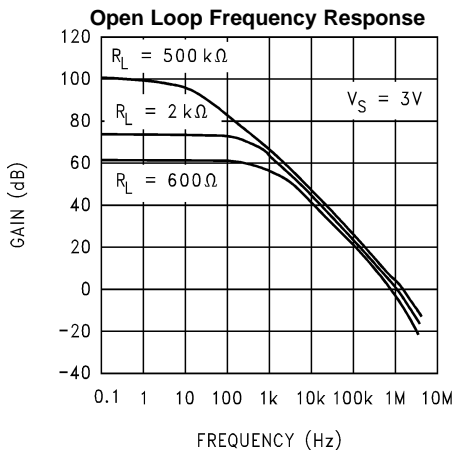


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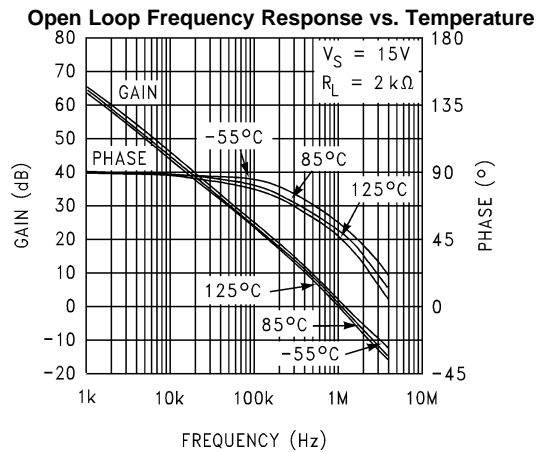


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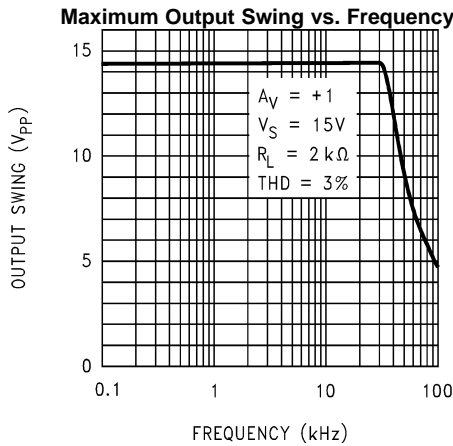


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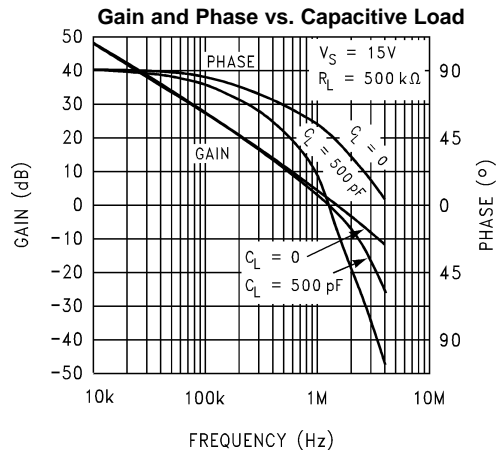
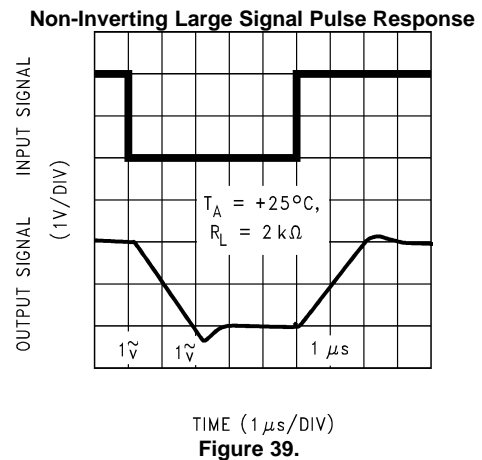
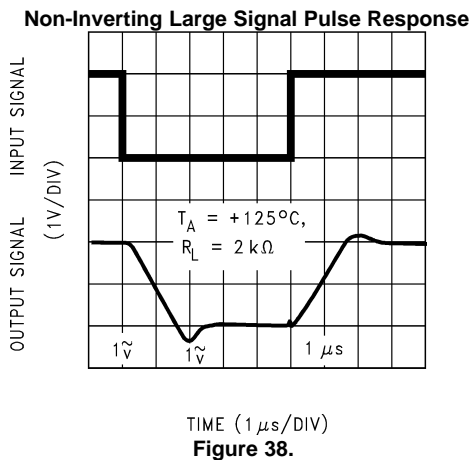
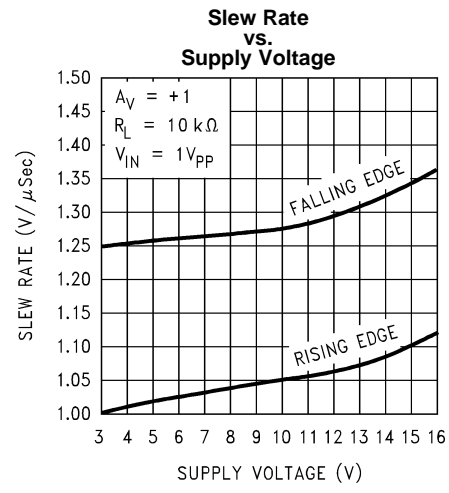
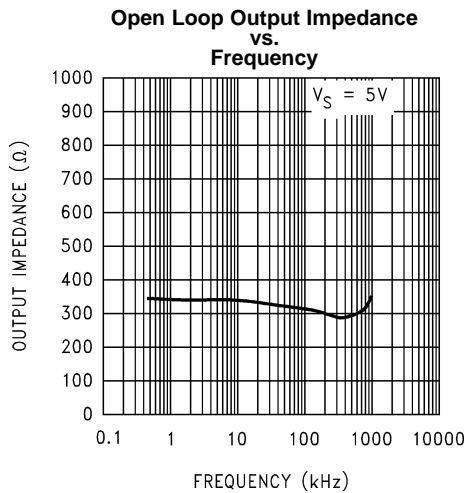
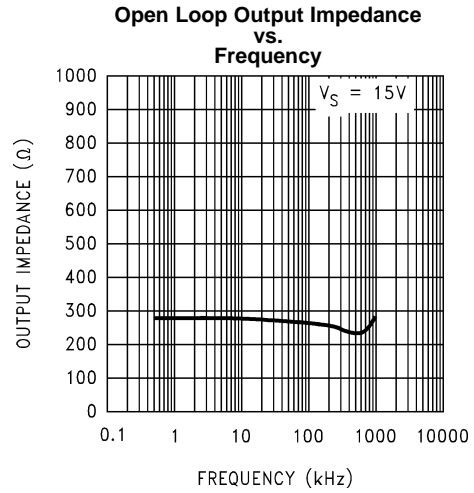
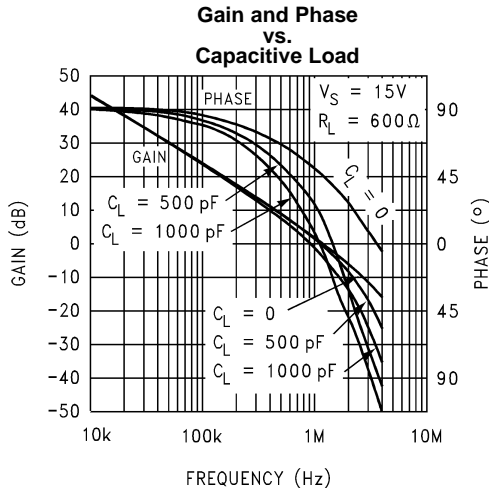


Figure 33.

**Typical Performance Characteristics (continued)**

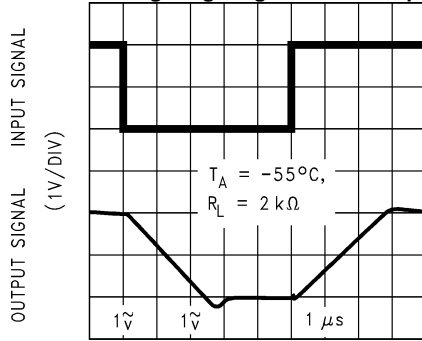
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Typical Performance Characteristics (continued)

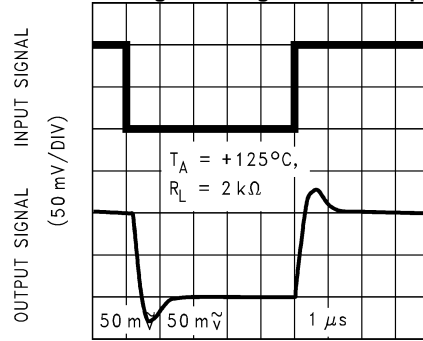
$V_S = +15V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

Non-Inverting Large Signal Pulse Response



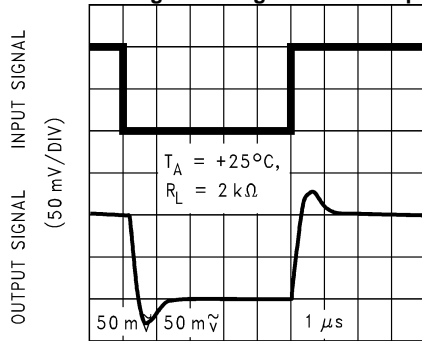
TIME (1 µs/DIV)  
Figure 40.

Non-Inverting Small Signal Pulse Response



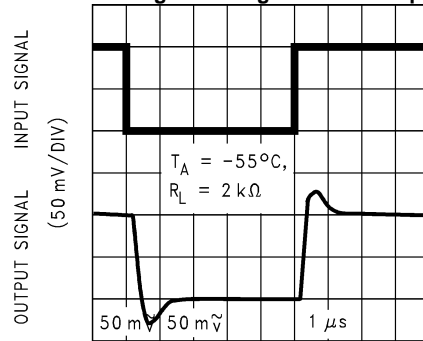
TIME (1 µs/DIV)  
Figure 41.

Non-Inverting Small Signal Pulse Response



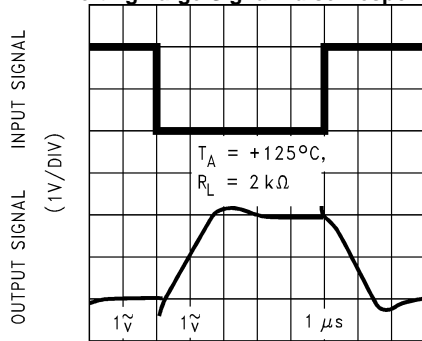
TIME (1 µs/DIV)  
Figure 42.

Non-Inverting Small Signal Pulse Response



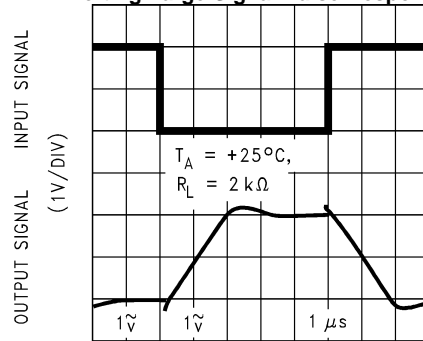
TIME (1 µs/DIV)  
Figure 43.

Inverting Large Signal Pulse Response



TIME (1 µs/DIV)  
Figure 44.

Inverting Large Signal Pulse Response

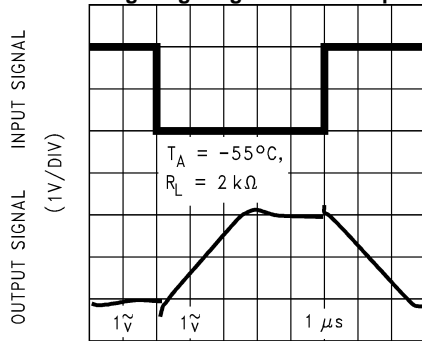


TIME (1 µs/DIV)  
Figure 45.

**Typical Performance Characteristics (continued)**

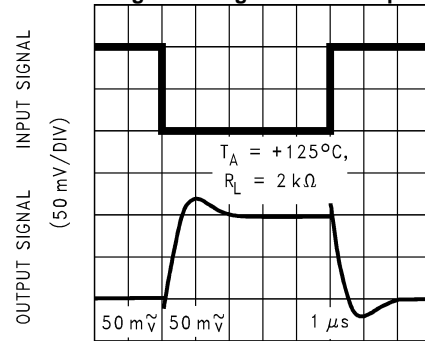
$V_S = +15V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

**Inverting Large Signal Pulse Response**



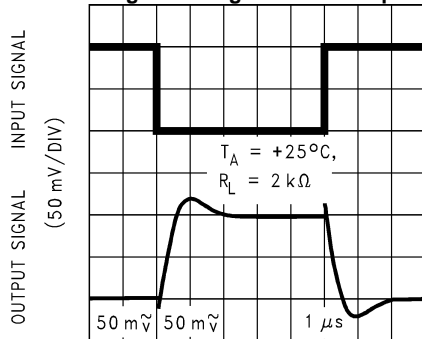
TIME ( $1 \mu s$ /DIV)  
**Figure 46.**

**Inverting Small Signal Pulse Response**



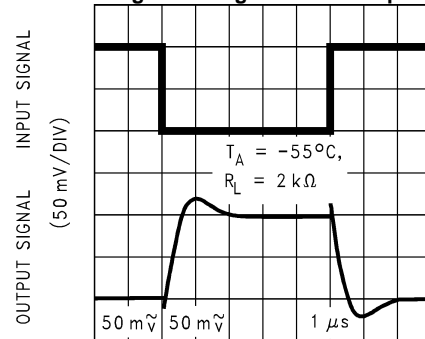
TIME ( $1 \mu s$ /DIV)  
**Figure 47.**

**Inverting Small Signal Pulse Response**



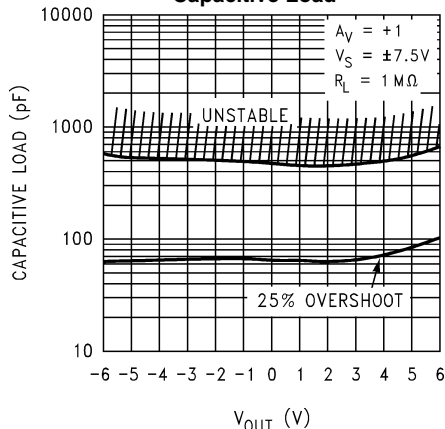
TIME ( $1 \mu s$ /DIV)  
**Figure 48.**

**Inverting Small Signal Pulse Response**



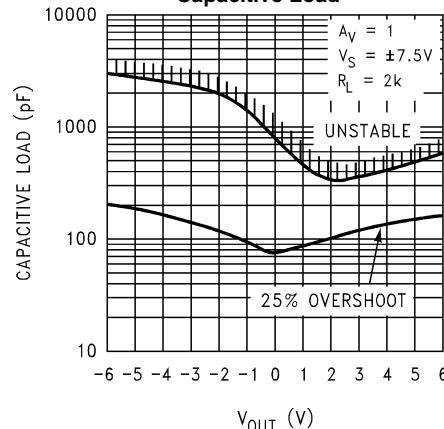
TIME ( $1 \mu s$ /DIV)  
**Figure 49.**

**Stability vs. Capacitive Load**



**Figure 50.**

**Stability vs. Capacitive Load**



**Figure 51.**

Typical Performance Characteristics (continued)

$V_S = +15V$ , Single Supply,  $T_A = 25^\circ C$  unless otherwise specified

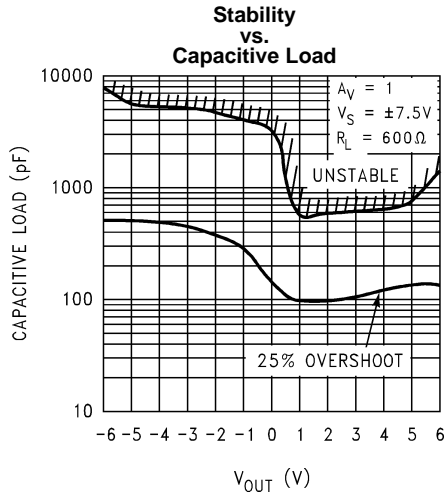


Figure 52.

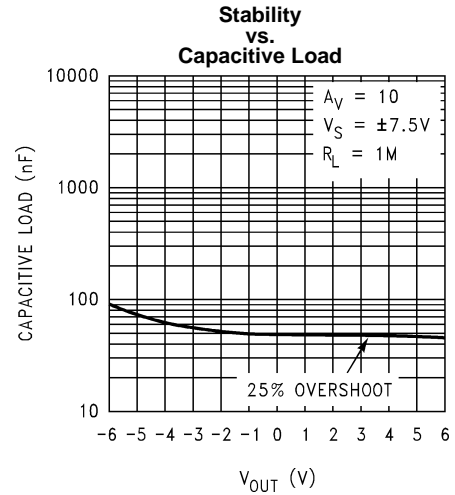


Figure 53.

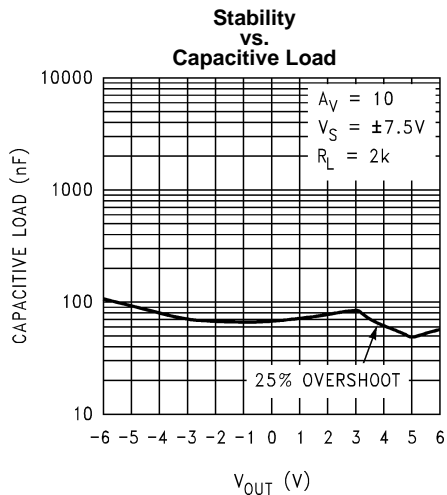


Figure 54.

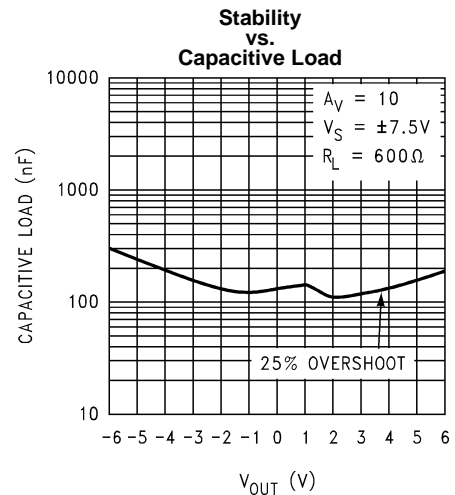


Figure 55.

## APPLICATION INFORMATION

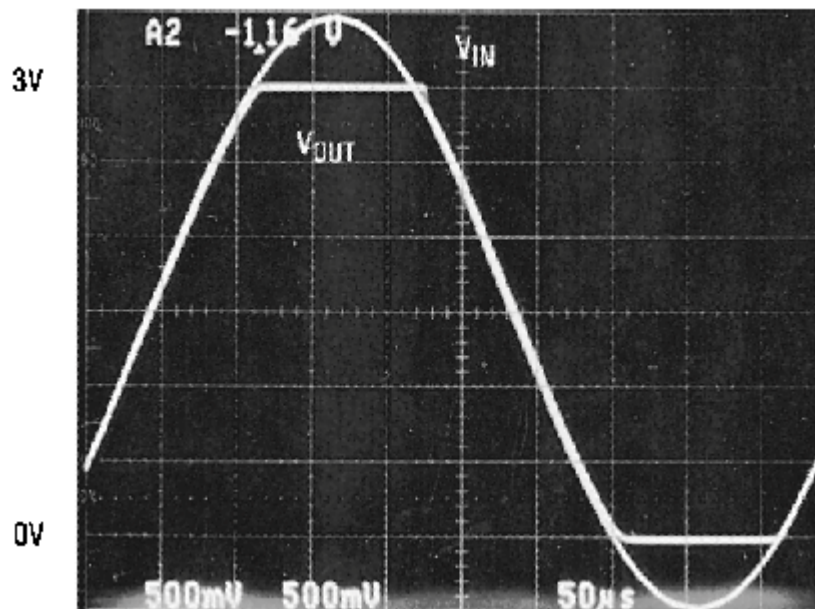
### AMPLIFIER TOPOLOGY

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6482's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

### INPUT COMMON-MODE VOLTAGE RANGE

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. [Figure 56](#) shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

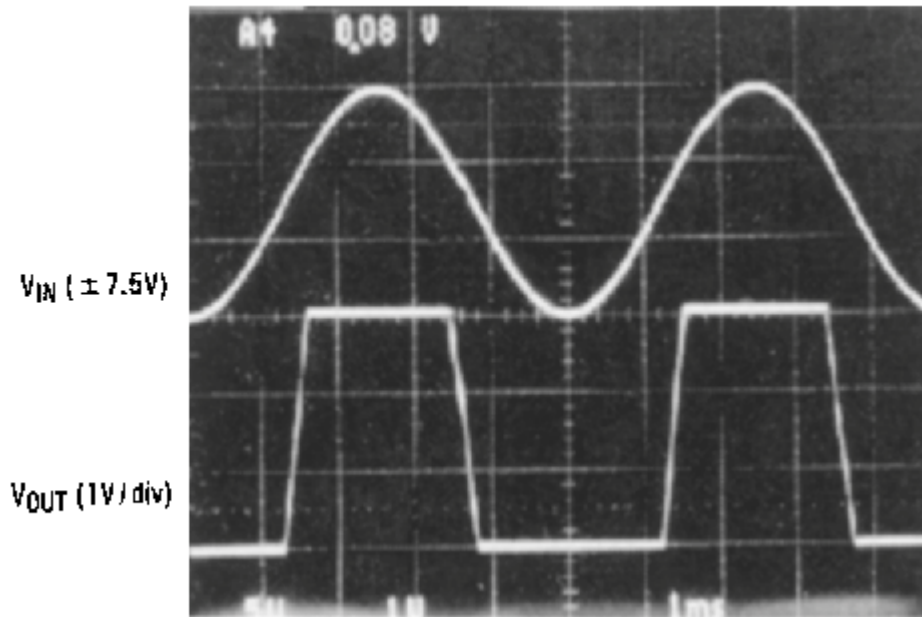


An input voltage signal exceeds the LMC6482 power supply voltages with no output phase inversion.

**Figure 56. Input Voltage**

The absolute maximum input voltage is 300mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in [Figure 57](#), can cause excessive current to flow in or out of the input pins possibly affecting reliability.

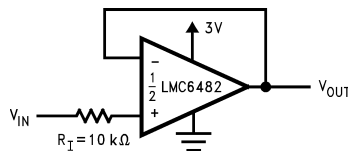




A  $\pm 7.5\text{V}$  input signal greatly exceeds the 3V supply in Figure 58 causing no phase inversion due to  $R_I$ .

**Figure 57. Input Signal**

Applications that exceed this rating must externally limit the maximum input current to  $\pm 5\text{mA}$  with an input resistor ( $R_I$ ) as shown in Figure 58.



$R_I$  input current protection for voltages exceeding the supply voltages.

**Figure 58.  $R_I$  Input Current Protection for Voltages Exceeding the Supply Voltages**

## RAIL-TO-RAIL OUTPUT

The approximated output resistance of the LMC6482 is  $180\Omega$  sourcing and  $130\Omega$  sinking at  $V_S = 3\text{V}$  and  $110\Omega$  sourcing and  $80\Omega$  sinking at  $V_S = 5\text{V}$ . Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

## CAPACITIVE LOAD TOLERANCE

The LMC6482 can typically directly drive a  $100\text{pF}$  load with  $V_S = 15\text{V}$  at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an under damped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 59. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

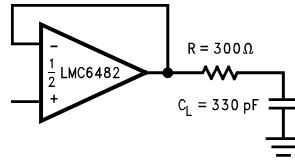


Figure 59. Resistive Isolation of a 330pF Capacitive Load

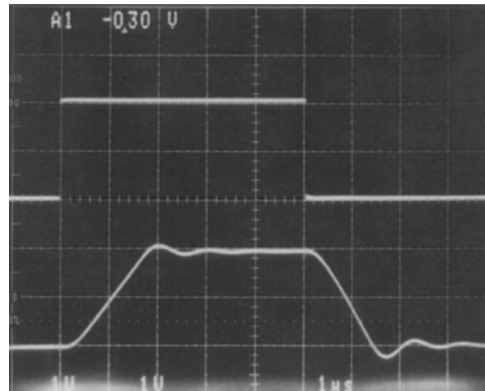
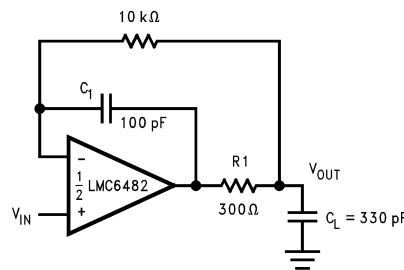


Figure 60. Pulse Response of the LMC6482 Circuit in Figure 59

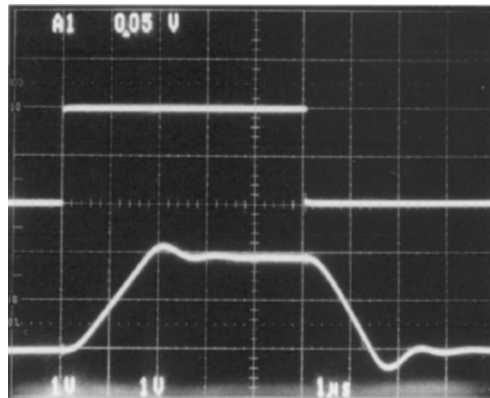
Improved frequency response is achieved by indirectly driving capacitive loads, as shown in Figure 61.



Compensated to handle a 330pF capacitive load.

Figure 61. LMC6482 Noninverting Amplifier

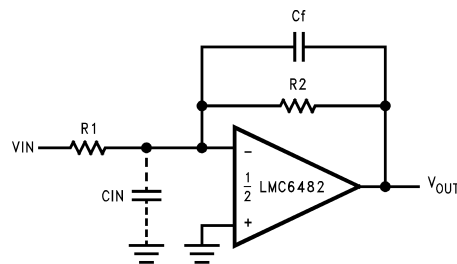
R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in Figure 62.



**Figure 62. Pulse Response of LMC6482 Circuit in Figure 61**

### COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photo diodes, and circuits board parasitics to reduce phase margins.



**Figure 63. Canceling the Effect of Input Capacitance**

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in [Figure 63](#)),  $C_f$ , is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

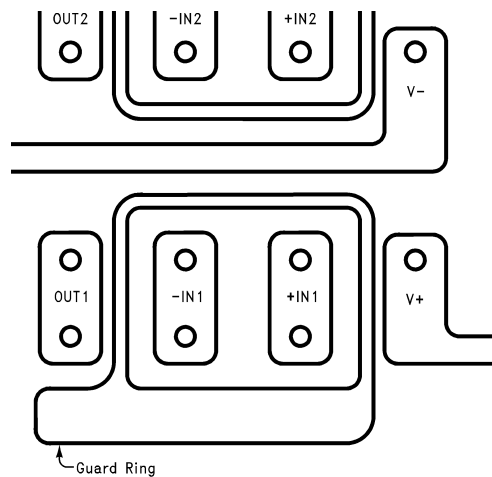
which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for  $C_f$  may be different. The values of  $C_f$  should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

## PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6482, typically less than 20fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in [Figure 64](#). To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of  $10^{12}\Omega$ , which is normally considered a very large resistance, could leak 5pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6482's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of  $10^{11}\Omega$  would cause only 0.05pA of leakage current. See [Figure 65](#) through [Figure 67](#) for typical connections of guard rings for standard op-amp configurations.



**Figure 64. Example of Guard Ring in P.C. Board Layout Typical Connections of Guard Rings**

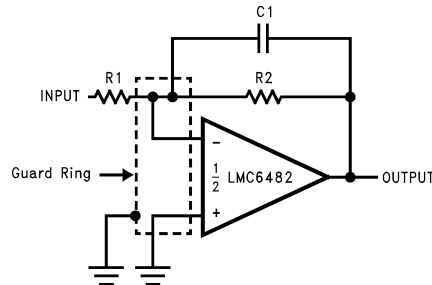


Figure 65. Inverting Amplifier Typical Connections of Guard Rings

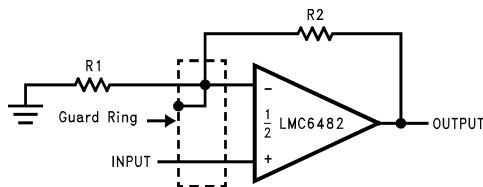


Figure 66. Non-Inverting Amplifier Typical Connections of Guard Rings

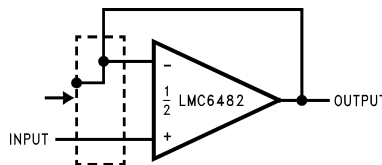
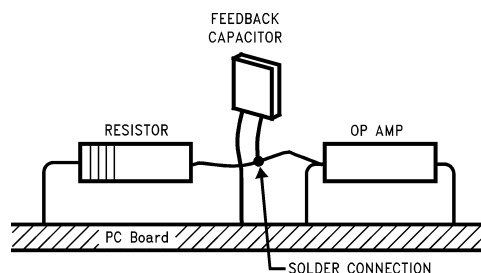


Figure 67. Follower Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 68](#).

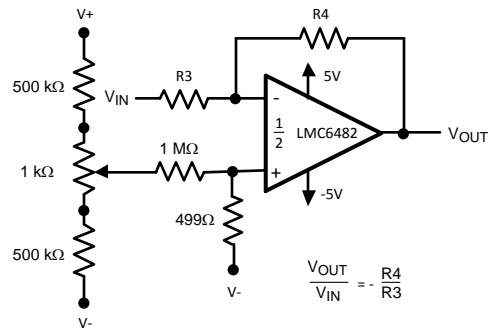


(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

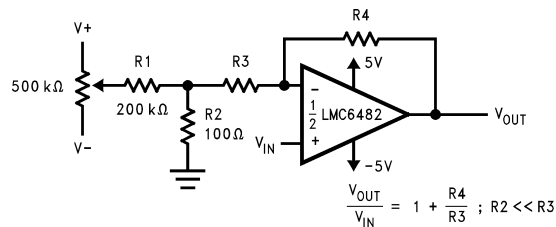
Figure 68. Air Wiring

## OFFSET VOLTAGE ADJUSTMENT

Offset voltage adjustment circuits are illustrated in [Figure 69](#) and [Figure 70](#). Large value resistances and potentiometers are used to reduce power consumption while providing typically  $\pm 2.5\text{mV}$  of adjustment range, referred to the input, for both configurations with  $V_S = \pm 5\text{V}$ .



**Figure 69. Inverting Configuration Offset Voltage Adjustment**



**Figure 70. Non-Inverting Configuration Offset Voltage Adjustment**

## UPGRADING APPLICATIONS

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6482's features. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

## DATA ACQUISITION SYSTEMS

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 (Figure 71). Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC4282 CMRR of 82dB maintains integral linearity of a 12-bit data acquisition system to  $\pm 0.325$  LSB. Other rail-to-rail input amplifiers with only 50dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.



Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

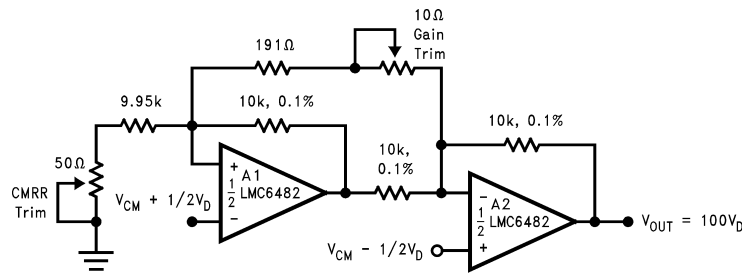


Figure 73. Low-Power Two-Op-Amp Instrumentation Amplifier

**SPICE MACROMODEL**

A spice macromodel is available for the LMC6482. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.

**Typical Single-Supply Applications**

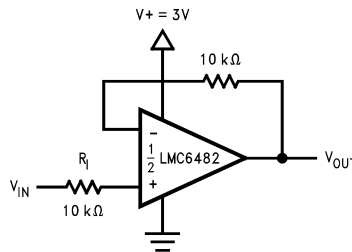


Figure 74. Half-Wave Rectifier with Input Current Protection (RI)

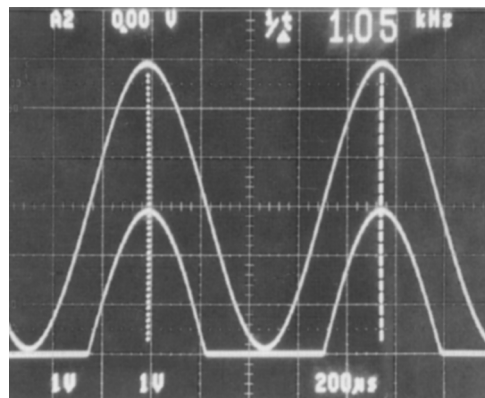


Figure 75. Half-Wave Rectifier Waveform



The circuit in Figure 74 uses a single supply to half wave rectify a sinusoid centered about ground.  $R_1$  limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in Figure 76.

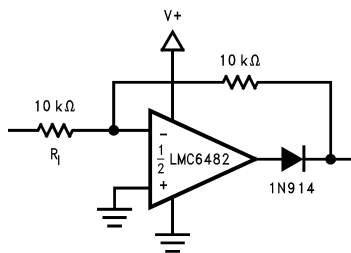


Figure 76. Full Wave Rectifier with Input Current Protection ( $R_1$ )

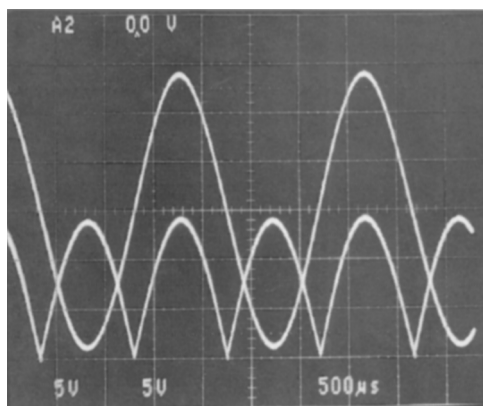


Figure 77. Full Wave Rectifier Waveform

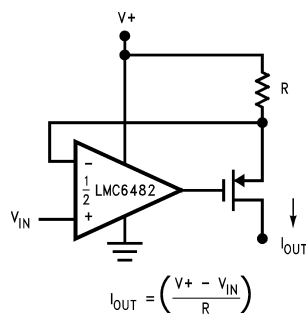


Figure 78. Large Compliance Range Current Source

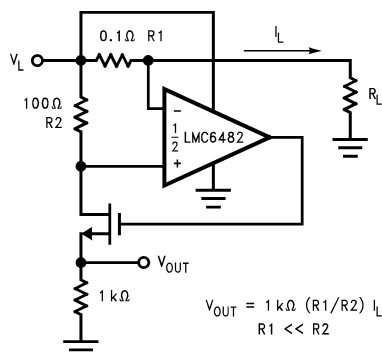
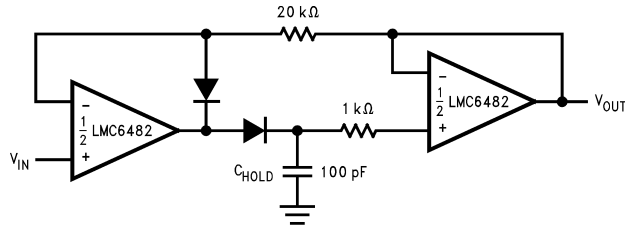
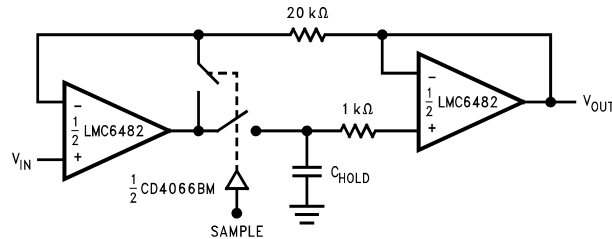


Figure 79. Positive Supply Current Sense



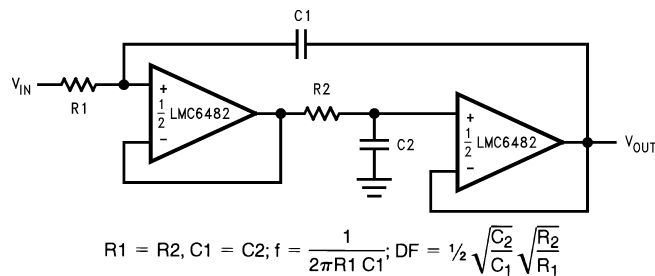
**Figure 80. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range**

In [Figure 80](#) dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of  $C_H$  and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.



**Figure 81. Rail-to-Rail Sample and Hold**

The LMC6482's high CMRR (82dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.



**Figure 82. Rail-to-Rail Single Supply Low Pass Filter**

The low pass filter circuit in [Figure 82](#) can be used as an anti-aliasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

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**REVISION HISTORY**

<b>Changes from Revision C (March 2013) to Revision D</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <a href="#">26</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC6482AIM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC6482AIM	<a href="#">Samples</a>
LMC6482AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6482AIM	<a href="#">Samples</a>
LMC6482AIMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC6482AIM	<a href="#">Samples</a>
LMC6482AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6482AIM	<a href="#">Samples</a>
LMC6482AIN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LMC6482AIN	<a href="#">Samples</a>
LMC6482AIN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85	LMC6482AIN	<a href="#">Samples</a>
LMC6482IM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC6482IM	<a href="#">Samples</a>
LMC6482IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6482IM	<a href="#">Samples</a>
LMC6482IMM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A10	<a href="#">Samples</a>
LMC6482IMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A10	<a href="#">Samples</a>
LMC6482IMMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	A10	<a href="#">Samples</a>
LMC6482IMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A10	<a href="#">Samples</a>
LMC6482IMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC6482IMX	<a href="#">Samples</a>
LMC6482IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6482IMX	<a href="#">Samples</a>
LMC6482IN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LMC6482IN	<a href="#">Samples</a>
LMC6482IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC6482IN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6482AIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482IMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6482AIMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482IMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6482IMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6482IMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6482IMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

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